

SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

5 The present invention relates to a semiconductor device containing a photoreception region comprising a photoelectric converter (for example, a solid state image sensor such as a CCD (charge-coupled device), CMOS (Complementary Metal-Oxide-Semiconductor) sensor, photodetector, etc.) in its integrated circuit.

10 This application is counterpart of Japanese patent applications, Serial Number 345641/2002, filed November 28, 2002, the subject matter of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

As conventional forms of packaging for a semiconductor device
15 containing a photoelectric converter (for example, a solid state image sensor, photodetector, etc.) in an integrated circuit, there are such packages as the so-called plastic package, and ceramic package. There is, for example, a package shown in Fig. 13 (refer to JP-A-2002-94035). This form of package has a case 70 made of plastics or ceramic, and external leads 72 protruding
20 from within the case 70 and extended on the exterior thereof. A single piece semiconductor chip 74 is housed inside the case 70, and a bonding wire 78 interconnects respective electrode pads 76 on top of the semiconductor chip

74 and respective internal ends of the external leads 72, disposed inside the case 70. A photoelectric converter (not shown) is formed in a photoreception region (integrated circuit) of the semiconductor chip 74, and a transparent cap 80 allowing light rays to pass therethrough is provided in a part of the 5 case 70, positioned above the photoreception region.

With the package of such a configuration as described above, however, since the external leads 72 are protruded from the outer wall of the case 70, a proportion of an extruded portion to the package in whole becomes large. This renders it difficult to use the package described above in a 10 device wherein a multitude of components need to be mounted in a small space, such as a mobile phone, handy camera, and so forth.

Due to recent trends toward such miniaturization of electronic equipment as described above, there has since been proposed a package called CSP (Chip Size Package) substantially identical in size to a 15 semiconductor chip in order to enable high density mounting of semiconductor devices to be implemented when mounting the semiconductor devices. However, there exists a problem in that the package proposed cannot be put to use as it is because in the case of a semiconductor device having a photoreception region, there is a need for depositing an insulator 20 layer, a redistribution wiring layer, and so forth, on top of the photoreception region.

With an object of overcoming such a problem, there has since been

proposed, for example, a semiconductor device (CSP) wherein connecting wiring is formed so as to extend from the surface of a semiconductor chip, on which an integrated circuit containing a photoreception region is formed, to a side face or the back face thereof in JP-A-2002-198463, A. With the 5 semiconductor device (CSP), since the connecting wiring is formed so as to extend from the surface of the semiconductor chip to the side face or the back face thereof, the semiconductor device can be surface mounted on, for example, a mounting board, and so forth such that the surface of the semiconductor device, with a photoreception region (integrated circuit) formed thereon, faces outside so as to enable photoreception, thereby 10 attaining ultra-compact mounting as a wafer level CSP.

Patent Document 1

JP-A-2002-94035

Patent Document 2

15 JP-2002-198463

However, it is to be pointed out that although the proposal described above has attained ultra-compact mounting, only an insulator layer is provided on the integrated circuit (photoreception region), although a form wherein a protection film is additionally formed on the integrated circuit is 20 also disclosed, insufficiency in respect of durability still remains at present when taking into consideration the fact that the same is handled as one component as packaged,

SUMMARY OF THE INVENTION

The invention has therefore been developed to overcome various problems encountered in the past, and is intended to attain the following 5 object. That is, the object of the invention is to provide a semiconductor device containing a photoreception region in its integrated circuit, having high durability while implementing ultra-compact mounting.

According to one aspect of the present invention, for achieving one or more of the above objects, there is provided a semiconductor device which 10 includes a semiconductor device includes a semiconductor chip having a main surface provided with an integrated circuit including a photoelectric converter and a first wiring for electrically connecting the integrated circuit of the semiconductor chip to respective external terminals. The semiconductor device also includes a sealing resin for sealing the main 15 surface of the semiconductor chip and the first wiring, formed so as to have an opening over the surface of the integrated circuit and a light-transmitting cap for covering the opening of the sealing resin.

BRIEF DESCRIPTION OF THE DRAWINGS

20 Fig. 1 is a schematic illustration showing the configuration of a first embodiment of a semiconductor device according to the invention, and Fig. 1 (A) is a plan view, Fig. 1 (B) being a sectional view;

Figs. 2 (A) through 2 (J) are schematic sectional views for illustrating a method of manufacturing the semiconductor device according to the first embodiment;

Fig. 3 is plan view showing another example of disposition positions 5 of solder balls in the semiconductor device according to the first embodiment;

Fig. 4 is a sectional view showing an example of a method of sealing with a sealing resin in the semiconductor device according to the first embodiment;

Fig. 5 is a sectional view showing another example of a method of 10 sealing with a sealing resin in the semiconductor device according to the first embodiment, and Fig. 5 (A) is a sectional view, Fig. 5 (B) being a plan view;

Fig. 6 is a sectional view showing still another example of a method of sealing with a sealing resin in the semiconductor device according to the first embodiment, and Fig. 6 (A) is a sectional view, Fig. 6 (B) being a plan 15 view;

Fig. 7 is a schematic illustration showing the configuration of a second embodiment of a semiconductor device according to the invention, and Fig. 7 (A) is a plan view, Fig. 7 (B) being a sectional view;

Fig. 8 is a schematic illustration showing the configuration of a 20 third embodiment of a semiconductor device according to the invention, and Fig. 8 (A) is a plan view, Fig. 8 (B) being a sectional view;

Fig. 9 is a schematic illustration showing the configuration of a

fourth embodiment of a semiconductor device according to the invention, and

Fig. 9 (A) is a plan view, Fig. 9 (B) being a sectional view;

Fig. 10 is a sectional view showing the configuration of a fifth embodiment of a semiconductor device according to the invention;

5 Fig. 11 is a schematic illustration showing the configuration of a camera module according to a sixth embodiment of the invention;

Fig. 12 is an enlarged schematic view for illustrating the disposition position of a sensor in the camera module according to the sixth embodiment of the invention; and

10 Fig. 13 is a schematic illustration showing the configuration of a conventional semiconductor device package.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of a semiconductor device according to the invention
15 are described hereinafter with reference to the accompanying drawings.

Parts having the same functions in effect are denoted by like reference numerals throughout figures, omitting description thereof in some cases.

First Embodiment

Fig. 1 is a schematic illustration showing the configuration of a first embodiment of a semiconductor device according to the invention, and Fig. 1 (A) is a plan view, Fig. 1 (B) being a sectional view. Figs. 2 (A) through 2 (J) are schematic sectional views for illustrating a method of manufacturing the

semiconductor device according to the first embodiment.

A semiconductor device 100 shown in Fig. 1 has a semiconductor chip 10 on which surface there is formed an integrated circuit (referred to as a photoreception region in some cases hereinafter because the integrated circuit herein contains a photoelectric converter: a region denoted by reference numeral 12 in the figure) containing a photoelectric converter (solid state image sensor such as, for example, a CCD (charge-coupled device), CMOS (Complementary Metal-Oxide-Semiconductor) sensor, photodetector, etc.). Electrodes 14 electrically continuous with the integrated circuit are formed on top of the semiconductor chip 10, and an insulator film (for example, a passivation film) 16 and a protection film (for example, a polyimide film) 18 are sequentially formed in part of the semiconductor chip 10, other than parts where the electrodes 14 are provided.

Further, with the semiconductor device 100, there are formed a redistribution wiring layer 20 extended from the respective electrodes 14, and bumps 22 for electrical connection with pads 24 for external connection, respectively, on the redistribution wiring layer 20. The bumps 22 are formed in the vicinity of the periphery of the integrated circuit, and are provided with a step 22a at respective tips thereof while the redistribution wiring layer 20 and the outer periphery of bumps 22, on the semiconductor chip 10, are sealed with a sealing resin 26 so as to have an opening over an

integrated circuit surface. A light-transmitting cap 30 is engaged with the step 22a at the respective tips of the bumps 22, and is disposed in such a way as to cover the opening in the sealing resin 26.

The light transmitting cap 30 can be made of glass, transparent resin, or the like, but may be made of material having the function of an ultraviolet cut filter. Further, if focusing on the photoreception region is possible, the light transmitting cap 30 may function as a lens.

A solder ball 28 serving as a terminal for external connection is formed on top of the respective pads 24 formed so as to be electrically connected to the respective bumps 22.

In the figure, the solder balls 28 are disposed so as to be arranged in two lines, but the invention is not limited thereto, so that the solder balls 28 may be disposed so as to be arranged in three lines as shown in Fig. 3.

Now, a process of manufacturing the semiconductor device 100 shown in Fig. 1 is described hereinafter by way of example.

First, there is prepared a wafer 32, on which an integrated circuit of an element serving as a semiconductor chip 10 is formed, after evaluation of electrical characteristics thereof {Fig. 2 (A)}. The protection film 18 is applied to portions of the wafer 32, where the insulator film over the electrodes 14 is removed, by the spin coater method, so forth, and the protection film 18 is etched by subjecting the same to exposure using a mask for contact with the respective electrodes 14 {Fig. 2 (B)}. The redistribution

wiring layer 20 as a base for forming wiring to be extended from the respective electrodes 14 and forming the bumps 22 is formed by sputtering, plating, and so forth {Fig. 2 (C)}.

Subsequently, in order to form the bumps 22, a resist is applied over 5 the wafer 32, and the resist is etched after subjecting the same to exposure using a mask, thereby forming openings in the resist. Thereafter, the bumps 22 are formed by plating, and so forth, and are cleaned after removing the resist {Fig. 2 (D)}. At this point in time, there is formed the step 22a, to which the light-transmitting cap 30 is fitted, at the tip of each of the bumps 10 22, and as a method of forming the steps 22a, there are suitably performed, for example, a method of removing only a portion of the tip of each of the bumps 22 by edging and a method (for example, a two-stage plating method) of forming the bumps 22 in two stages, whereby the bumps 22 are formed to a predetermined height in a first stage and subsequently, an addition to the 15 respective bumps 22, corresponding to only a portion of the respective tips thereof, is formed in the next stage.

Next, the redistribution wiring layer 20 and the outer periphery of 20 bumps 22 are sealed with the sealing resin 26 so as to define an opening over an integrated circuit surface {Fig. 2 (E)}. In this case, as a method of sealing with the sealing resin 26 so as to define the opening over the integrated circuit surface, there is cited, for example, a method of employing a jig 34 covering the wafer 32 in whole and having a protruded part 34a on

the surface thereof as shown Fig. 4. With this method, the jig 34 is placed such that the protruded part 34a is fitted into an integrated circuit forming region so as to be butted against the sidewall of the bumps 22 and the steps 22a as well as the integrated circuit surface, and the sealing resin 26 in 5 liquid state is injected through a gap between the wafer 32 and the jig 34, that is, from horizontal sides of the wafer 32 (as indicated by the arrows in the figure) before sealing. Alternatively, there are suitably performed other methods such as a method of sealing by dropping the sealing resin 26 in liquid state from the top surface of the wafer 32 with the use of the jig 36 to 10 be fitted into the integrated circuit forming region so as to be butted against the sidewall of the bumps 22 and the steps 22a as well as the integrated circuit surface, before sealing, as shown in Fig. 5, and a method of sealing by dropping the sealing resin 26 in liquid state from the top surface of the wafer 32 with the use of a frame 38 having protrusions for stopping up a gap 15 between the bumps 22, adjacent to each other, of a plurality of the bumps 22 formed on the periphery of the integrated circuit, as shown in Fig. 6. Furthermore, there is also cited a method (not shown) of sealing by sealing the entire surface of the wafer 32 once with the sealing resin 26, and subsequently, by forming an opening in the integrated circuit forming region 20 after etching by use of photolithographic techniques and so forth before sealing.

After sealing with the sealing resin 26, an upper portion thereof is

cut by a grinder 40, and so forth (cutting tool, grindstone, buff, etc.) from the upper surface of the wafer 32, and the surface of the sealing resin 26 is ground (surface grinding), thereby exposing the bumps 22 hidden by the sealing resin 26 {Fig. 2 (F)}.

5 Subsequently, the light-transmitting cap 30 is fitted to the step 22a at the tip of each of the bumps 22, thereby covering the opening of the sealing resin 26 {Fig. 2 (G)}.

Thereafter, the pads 24 are formed on the respective tips of the bumps 22, and on parts of the periphery of the light-transmitting cap 30 by 10 sputtering or plating {Fig. 2 (H)}, further, the solder ball 28 is formed on top of the respective pads 24 {Fig. 2 (I)}, and finally, the wafer 32 is scribed into individual pieces after testing, thereby obtaining the respective semiconductor devices 100 {Fig. 2 (J)}.

The semiconductor device 100 according to the present embodiment 15 is configured such that the redistribution wiring layer 20 and the bumps 22, on the periphery of integrated circuit, are sealed with the sealing resin 26, and the light-transmitting cap 30 is provided above (in the direction normal to the integrated circuit surface) the integrated circuit (photoreception region) so as to be packaged in a size substantially equivalent to that of the 20 semiconductor chip 10. With the light-transmitting cap 30 being provided, light can shine on the photoreception region (integrated circuit) while the integrated circuit on the semiconductor chip 10 is shielded from outside.

Hence, even with the semiconductor device containing the photoreception region in the integrated circuit, durability thereof can be enhanced while implementing ultra-compact mounting.

Further, with the present embodiment, since the light-transmitting cap 30 is disposed so as to be fitted to the step 22a at the respective tips of the bumps 22 formed in the vicinity of the periphery of the integrated circuit, misalignment in positioning of the light-transmitting cap 30 is not prone to occur by virtue of the steps 22a, so that the semiconductor device is insusceptible to the adverse effect of impact, and the like, and durability is thereby enhanced.

In addition, with the present embodiment, blanket processing in wafer state is possible in almost every step of a manufacturing method, that is, manufacturing making use of a wafer level CSP technology can be implemented, so that reduction in cost can be attained.

15 Second Embodiment

Fig. 7 is a schematic illustration showing the configuration of a second embodiment of a semiconductor device according to the invention, Fig. 7 (A) is a plan view, and Fig. 7 (B) a sectional view.

The semiconductor device according to the second embodiment is the same in configuration as the semiconductor device according to the first embodiment except that a protection film 18 having an opening 18a over an integrated circuit (photoreception region) is provided. As a method of

providing the protection film18 with the opening 18a, there are available a method of selectively forming the protection film18 by use of a mask at the time of forming the protection film18 {refer to Fig. 2 (B)} in the process of manufacturing the semiconductor device as described in the first 5 embodiment, thereby defining the opening 18a, a method of forming the redistribution wiring layer 20 {refer to Fig. 2 (C)}, and subsequently, defining the opening 18a by etching a portion of the redistribution wiring layer 20, in the integrated circuit forming region, by photolithographic techniques, and so forth.

10 When resin films having high dielectric constant (in the case of the first embodiment, the insulator film 16 and the protection film18) exist in the vicinity of a circuit, electric current normally has difficulty in flowing through the circuit. The reason for this is because the resin films (the dielectric constant of resin is normally about 4) having high dielectric 15 constant block a magnetic field generated upon electric current flowing through the circuit, resulting in an increase in resistance of the circuit.

With the present embodiment, therefore, a portion of the protection film18 among the resin films existing in the vicinity of integrated circuit, contributing to an increase in resistance, is removed, thereby causing the 20 dielectric constant thereof to approach that of air, that is, 1, as much as possible, so that the semiconductor device can better cope with high speed RF.

Third Embodiment

Fig. 8 is a schematic illustration showing the configuration of a third embodiment of a semiconductor device according to the invention, Fig. 8 (A) is a plan view, and Fig. 8 (B) a sectional view.

5 With the semiconductor device according to the third embodiment, a light-transmitting cap 30 is made up of a portion of a wiring board 30a, and a cap 30b assembled into the central part of the wiring board 30a. Wiring 30c causing electrically continuity between the top surface and the back side by forming a through hole or the like for electrically connecting respective 10 bumps 22 with respective pads 24 is provided on the periphery of the wiring board 30a. The wiring 30c is formed in the same wiring pattern as that for an ordinary printed wiring board. Further, the wiring board 30a may be of a multiplayer wiring structure. The light-transmitting cap 30 can be made with ease by, for example, defining an opening at the central part of the 15 wiring board 30a provided with any suitable wiring pattern, and provided with a protection film of a solder resist, and so forth, formed thereon, and by fitting the cap 30b into the opening.

20 The light-transmitting cap 30 (the wiring board 30a) is connected with the respective bumps 22 by, for example, forming terminals on the wiring board 30a by use of tin plating, and so forth, and by thermal compression bonding of each of the terminals with the respective bumps 22. Then, as with the case of the first embodiment, pads 24 are formed so as to

be electrically connected with the wiring 30c of the wiring board 30a by sputtering, plating, and so forth.

With the present embodiment, since the light-transmitting cap 30 is made up such that a portion thereof is the wiring board 30a provided with a

5 wiring pattern beforehand, there is an increase in flexibility in respect of disposition position (formation position) of the respective bumps 22 (solder balls 28).

Furthermore, with the present embodiment, since the light-transmitting cap 30 made up of the wiring board 30a provided with the 10 wiring pattern beforehand is employed, blanket processing in wafer state is possible in almost every step of a manufacturing method, that is, manufacturing making use of the wafer level CSP technology can be implemented, so that reduction in cost can be attained.

In addition, with the present embodiment, if the wiring board 30a is 15 provided with the bumps 22 beforehand, it is possible to omit a processing step of forming the bumps 22 as described in the first embodiment {Fig. 2 (H)}, so that further reduction in cost can be attained.

Fourth Embodiment

Fig. 9 is a schematic illustration showing the configuration of a 20 fourth embodiment of a semiconductor device according to the invention, Fig. 9 (A) is a plan view, and Fig. 9 (B) a sectional view.

The semiconductor device according to the fourth embodiment is the

same in configuration as the semiconductor device according to the third embodiment except that a protection film 18 having an opening 18a over an integrated circuit (photoreception region) is provided.

With the present embodiment, a portion of the protection film 18 among the resin films existing in the vicinity of integrated circuit, contributing to an increase in resistance, is removed, thereby causing the dielectric constant to approach that of air, that is, 1, as much as possible, so that the semiconductor device can better cope with high speed RF as with the case of the second embodiment.

10 Fifth Embodiment

Fig. 10 is a sectional view showing the configuration of a fifth embodiment of a semiconductor device according to the invention.

The present embodiment is configured such that a light-transmitting resin such as, for example, an epoxy resin etc. is used for a sealing resin 26, and the entire top surface of a semiconductor chip 10 is sealed with the sealing resin 26.

The semiconductor device according to the present embodiment is made up such that the entire top surface of the semiconductor chip 10 is sealed with the sealing resin 26 having a light-transmitting property, and the semiconductor device is packaged in a size substantially equivalent to that of the semiconductor chip 10. With the use of the sealing resin 26 having the light-transmitting property for sealing, light can shine on the

photoreception region (integrated circuit) while shielding the integrated circuit on the semiconductor chip 10 from outside. Hence, even with the semiconductor device containing the photoreception region in the integrated circuit, durability thereof can be enhanced while implementing 5 ultra-compact mounting.

Further, the semiconductor device according to the present embodiment adopts a configuration wherein sealing is implemented by the sealing resin 26 having the light-transmitting property, so that the thickness of films can be further reduced in comparison with the case of the first 10 embodiment.

In addition, with the present embodiment, processing steps of forming the step 22a for each of the bumps 22, and fitting the light-transmitting cap 30 into the opening can be omitted, so that further reduction in cost can be attained in comparison with the case of the first 15 embodiment.

Sixth Embodiment

Fig. 11 is a schematic illustration showing the configuration of a camera module according to a sixth embodiment of the invention.

A camera module (optical apparatus) 50 comprises a lens 56, a 20 sensor 52 disposed in a rearward position along the optical axis, a DSP (Digital Signal Processor) 54 for executing predetermined digital signal processing against digital signals as inputted, and a case 58. The sensor 52

and the DSP 54 are mounted on a mounting board 60, and as shown in Fig. 12, the sensor 52 is mounted such that a photoreception region (integrated circuit) thereof is opposed to the side of the mounting board 60 so as to receive light rays through an opening 60a provided in the mounting board 60.

5 Further, although not shown in the figure, the sensor 52 is connected to the DSP 54 through the intermediary of an analog/digital converter for converting analog signals as inputted into digital signals. In the figures, other constituent members and wiring are omitted for the sake of brevity.

With the present embodiment, the semiconductor device 100 according to any of the first through fifth embodiments is applied thereto as the sensor 52 of the camera module of such a configuration as described. Hence, ultra-compact mounting of the sensor 52 can be implemented, so that it becomes possible to attain down-sizing of the camera module, and to enhance durability thereof.

15 Thus, the camera module according to the present embodiment is suitably applicable to an electronic equipment making advances in miniaturization, such as mobile phone, handy camera, and so forth.

Now, it is to be understood that any of the preferred embodiments of the invention, described above, should not be construed as limiting the scope 20 of the invention, and obviously, various changes and modifications may be made without departing from the spirit and scope of the invention.

As described in the foregoing, with the semiconductor device

according to the invention, containing the photoreception region in the integrated circuit thereof, high durability can be ensured while implementing ultra-compact mounting.

While the preferred form of the present invention has been
5 described, it is to be understood that modifications will be apparent to those skilled in the art without departing from the spirit of the invention. The scope of the invention is to be determined solely by the following claims.